library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity DMUX1\_8 is

Port (i: in bit;

s: in bit\_vector(2 downto 0);

y: out bit\_vector(7 downto 0));

end DMUX1\_8;

architecture Behavioral of DMUX1\_8 is

begin

y(0) <= i when s = "000" else '0';

y(1) <= i when s = "000" else '0';

y(2) <= i when s = "000" else '0';

y(3) <= i when s = "000" else '0';

y(4) <= i when s = "000" else '0';

y(5) <= i when s = "000" else '0';

y(6) <= i when s = "000" else '0';

y(7) <= i when s = "000" else '0';

end Behavioral;